

IN THE CLAIMS:

Please delete the paragraph heading on page 12 of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please insert the paragraph heading on page 12 of the subject application, before claim 1, the following:

-- What is claimed is: --.

Please amend the claims as follows:

1. (Currently Amended) Method for producing a semiconductor device with the steps of:
 - (a) applying an interconnect level (11, 12) to a semiconductor substrate (10);
 - (b) structuring the interconnect level (11, 12); and
 - (c) applying a solder layer (13) on the structured interconnect level (11, 12) in such a way that the solder layer (13) assumes the structure of the interconnect level (11, 12).
2. (Currently Amended) Method according to claim 1, ~~characterized in that~~ wherein the interconnect level (11, 12) is applied in a sputtering process or in a depositing process without external current.
3. (Currently Amended) Method according to claim 1 ~~or 2, characterized in that, wherein~~ the interconnect level (12) which is applied comprises a metal, preferably copper and/or nickel and/or aluminum.
4. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the interconnect level (11, 12) is structured with the aid of a photolithographic process.
5. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein a carrier layer (11) which preferably comprises titanium and is structured like the interconnect level (12) is applied on the semiconductor substrate (10).
6. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the solder layer (13) is applied in a printing process and is distributed in a predetermined way by re-liquefying or reflowing of the solder.

7. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the solder layer (13) is applied in a dip soldering process, in which the upper side of the semiconductor substrate (10) provided with the structured interconnect level (11, 12) is dipped into a solder bath.
8. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein a solder resist layer is selectively applied on predetermined portions of the arrangement after the structuring of the interconnect level (11, 12) and before the application of the solder layer (13).
9. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein side walls (16) of the structured interconnect level (11, 12) and/or of the carrier layer (14) are wetted with solder.
10. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein both solder traces and solder balls (30) for the bonding of further semiconductor devices and/or a printed circuit board in the vertical direction are formed during the application of the solder layer (13), preferably in the same process step.
11. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein, after the application of the structured solder layer (13), a non-conductive plastic, preferably polymer, is applied in such a way that the tips of the solder balls (30) for the vertical bonding protrude from the plastic, other solder structures being covered over.
12. (Currently Amended) Method according to claim 11, ~~characterized in that~~ wherein the applied polymer is only cured during or after the electrical bonding with a further semiconductor device and/or a printed circuit board in the vertical direction.
13. (Currently Amended) Method according to claim 11 ~~or 12, characterized in that~~, wherein the polymer is applied in a printing process.
14. (Currently Amended) Method according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the conductive interconnect level (12) is formed on the semiconductor substrate (10) and/or contact devices such as bonding pads in a printing or stamping process with a highly reactive

- substance, which comprises at least one noble metal, such as preferably platinum or palladium.
15. (Currently Amended) Semiconductor device with:
- (a) a semiconductor substrate (10);
 - (b) a structured interconnect level (11, 12) on the semiconductor substrate (10); and
 - (c) a solder layer (13) on the structured interconnect level (11, 12) for enlarging the conductive cross section, the solder layer (13) assuming the structure of the interconnect level (11, 12).
16. (Currently Amended) Semiconductor device according to claim 15, characterized in that wherein the structured interconnect level (12) comprises a metal, in particular aluminum and/or copper.
17. (Currently Amended) Semiconductor device according to claim 15 ~~or 16~~, characterized in that, wherein the structured interconnect level (11, 12) provides on the semiconductor substrate (10) a carrier layer (11), which is structured like the interconnect level (12) and preferably comprises titanium and/or copper.
18. (Currently Amended) Semiconductor device according to ~~one of claims 15 to 17~~, characterized in that claim 15, wherein side walls (16) of the structured interconnect level (11, 12) and/or of the carrier layer (11) are wetted with solder.
19. (Currently Amended) Semiconductor device according to ~~one of claims 15 to 18~~, characterized in that claim 15, wherein the semiconductor device is mechanically connected to at least one further semiconductor device and/or a printed circuit board by means of a plastic or a polymer, the electrical connection being provided in the vertical direction by means of solder balls (30).
20. (Currently Amended) Semiconductor device according to ~~one of claims 15 to 19~~, characterized in that claim 15, wherein the structured solder layer (13) has a solder layer height (14, 24) which corresponds approximately to half the structure width (15, 25) of the structured interconnect level (12).